

REMARKS

This is in response to the Office Action dated March 2, 2004. Claims 16-23 are pending.

With respect to the formality issues raised on page 2 of the Office Action, it is respectfully submitted that the claim changes herein address and overcome any potential formality issue in this regard.

General

For purposes of example, and without limitation, certain example embodiments of this invention relate to a semiconductor device having a structure which allows for easier processing and alignment during the manufacture thereof. For example, Fig. 1 of the instant application illustrate a semiconductor device including *metal* gate electrode 19, gate insulator 13, respective *metal* contact plugs 20 provided over S/D regions 15, and interlayer insulator 22 provided over both the gate electrode 19 and isolation regions 12 (e.g., see especially Figs. 1(f) – 1(j)). *The metal gate electrode 19 directly contacts an upper surface of the gate insulating film 13 so that only the gate insulating film 13 is located between the metal gate electrode 19 and a channel of a transistor for which the gate electrode is provided.* The gate electrode 19 is electrically isolated from the contact plugs 20 by the sidewall insulating film(s) 16, and the gate electrode 19 and the contact plugs 20 both have the same height as best shown in Fig. 1(i). *Since the gate electrode 19 and contact plugs 20 are both formed of metal, they advantageously may both be formed in the same process step using the same material.* This unique structure is

advantageous in that it allows an easier process of manufacture as explained above and also permits contact plugs 20 to be formed in the vicinity of the gate electrode 19 in a self-aligned manner, so that electrical isolation between the gate electrode 19 and contact plugs 20 is ensured for prevention of a short between the gate electrode and the contacts of the interconnection (e.g., pgs. 24-25). Further, the contact plugs 20 can be spaced by a minimum distance from the gate electrode 19 as desired by adjusting the thickness of the sidewall insulating film 16. Therefore, the contacts can be provided close to the gate electrode, whereby a parasitic resistance in the source/drain regions can be reduced for improvement of the device characteristics of the transistor (e.g., pg. 25).

Claim 16

Claim 16 stands rejected under 35 U.S.C. Section 102(b) as being allegedly anticipated by Fuller (newly cited). This Section 102(b) rejection is respectfully traversed for at least the following reasons.

Claim 16 requires "a metal gate electrode provided on a semiconductor substrate with the intervention of a gate insulating film, wherein the metal gate electrode directly contacts an upper surface of the gate insulating film so that only the gate insulating film is located between the metal gate electrode and a channel of a transistor for which the gate electrode is provided; a sidewall insulating film provided on a side wall of the metal gate electrode; source/drain regions provided in the semiconductor substrate for the transistor, the channel being provided between the source/drain regions; metal contact plugs provided on the source/drain regions; wherein the metal gate electrode is

electrically isolated from the metal contact plugs by the sidewall insulating film alone; wherein the metal gate electrode is partly or entirely composed of the same material as the metal contact plugs; wherein the metal gate electrode and the metal contact plugs have the same height." For purposes of example only, Fig. 1 illustrates that the metal gate electrode 19 directly contacts an upper surface of the gate insulating film 13 so that only the gate insulating film 13 is located between the metal gate electrode 19 and a channel of a transistor for which the gate electrode is provided. Moreover, the metal gate electrode 19 is partly or entirely composed of the same material as the metal contact plugs 20 which are isolated from the gate electrode via insulator(s) 16; and the metal gate electrode 19 and the metal contact plugs 20 have the same height.

Fuller fails to disclose or suggest the aforesaid underlined aspect of claim 16. Fuller in Figs. 2E-2F discloses polysilicon gate electrode 211, source/drain regions 213/214, and gate insulator 215, and insulating gate sidewall spacers 221. As shown in Figs. 2D-2E of Fuller, a tungsten layer 223 is deposited over the gate and source/drain regions of the transistor and is thereafter planarized so that tungsten portion 231 is provided over the gate and tungsten portions 232, 233 are provided over the source/drain regions (e.g., col. 4, lines 20-55).

However, in contrast with Fuller, claim 16 as amended requires that "*the metal gate electrode directly contacts an upper surface of the gate insulating film so that only the gate insulating film is located between the metal gate electrode and a channel of a transistor.*" Fuller fails to disclose or suggest this aspect of claim 16 in view of Fuller's

requirement for polysilicon (non-metal) gate electrode 211. Fuller teaches directly away from the invention of amended claim 16 by requiring non-metal gate electrode 211. Moreover, because of Fuller's use of a non-metal gate electrode, Fuller's structure is highly undesirable because it requires an additional non-metal layer 211 in between the gate insulator 215 and metal 231 thereby adding significant costs and processing requirements to the overall device. In other words, Fuller cannot possibly form the gate electrode 211 and the alleged plugs 232, 233 all in the same step because they are of much different materials – Fuller is highly undesirable in this regard.

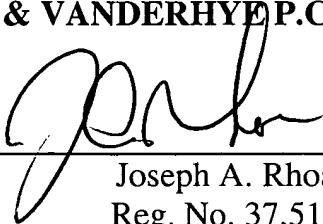
Conclusion

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____


Joseph A. Rhoa
Reg. No. 37,515

JAR:caj
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100